

What is claimed is:

1. A method of forming a gate in a semiconductor device comprising the steps of:

- 5 forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;
- depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially;
- 10 patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer using the mask pattern as an etch barrier;
- forming spacers at both sidewalls of the dummy gate polysilicon layer;
- 15 depositing an insulating interlayer on the resultant structure after forming the spacers;
- exposing a surface of the dummy gate polysilicon layer by carrying out an oxide layer CMP process having a high selection ratio against the dummy gate polysilicon layer;
- 20 forming a damascene structure by removing the dummy gate polysilicon layer and the dummy gate insulating layer using the insulating interlayer

as another etch barrier;
depositing a gate insulating layer and a gate metal
layer on the entire surface of the semiconductor
substrate having the damascene structure; and
5 exposing a surface of the insulating interlayer by
carrying out a metal chemical mechanical polishing
process having a high selection ratio against the
insulating interlayer.

10 2. The method of claim 1, wherein the dummy gate
polysilicon layer is formed to a thickness of from
1300 to 2000 Å.

15 3. The method of claim 1, wherein the insulating
interlayer is formed to a thickness of from 4000
to 5000 Å.

20 4. The method of claim 1, wherein the polishing
selection ratio between the insulating interlayer
and the dummy gate polysilicon layer is maintained
over 20.

5. The method of claim 1, wherein the insulating
interlayer chemical mechanical polishing uses a

slurry including CeO_2 particles.

6. The method of claim 5, wherein the pH of the slurry, including CeO_2 particles, is set between 3 and 11.

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7. The method of claim 1, wherein the polishing selection ratio between the insulating interlayer and the gate metal layer is maintained over 50.

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8. The method of claim 1, wherein the metal chemical mechanical polishing uses slurry for a metal layer.

9. The method of claim 8, wherein the pH of the slurry for a metal layer is set between 2 and 7.

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